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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,475	10/29/2003	Chan-Yong Kim	8836-206 (IB12280-US)	7422

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Frank Chau
F. CHAU & ASSOCIATES, LLP
Suite 501
1900 Hempstead Turnpike
East Meadow, NY 11554

EXAMINER	
NGUYEN, HIEP	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 07/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Acti n Summary	Application No.	Applicant(s)	
	10/697,475	KIM, CHAN-YONG	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disp sition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5-7 and 11* is/are rejected.

7)☒ Claim(s) *2-4 and 8-10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 1 is objected to because of the following informalities: It is not clear as to the recitation "the reference voltage signal" on line 8 is the same or different than the " a reference voltage " on line 4. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 5, 6, 7 and 11 are rejected under 35 U.S.C. 102 (e) as being anticipated by Cyrusian et al. (US Pat. 6,697,205).

Regarding claims 1 and 5, figure 2 and 3 of Cyrusian show a temperature detection circuit comprising:

an op- amp (316) for receiving a band gap reference voltage (320) and a first voltage (328);

a reference current generator (312, 414, 318) for generating the first voltage at node (328) and a reference voltage (V3 at node 322) in response to an output signal of the op-amp;

a temperature detection voltage generator (308, 304 and 232, 234 in figure 2) for generating a temperature detection voltage (V4) at node (324) in response to an ambient temperature and the output signal (330) of the op-amp (note that amplifier 316 generates current I1 that creates a reference voltage V3 at node 322); and

a comparator (306) for comparing the reference voltage signal (V3) with the temperature detection voltage signal (V4) to generate a temperature control signal (Vb2). Note that transistors (232, 234) sense the change of temperature. The impedance of transistor (308) changes according to the temperature and the temperature control signal (Vb2) is generated (col. 8, lines 10-20). The sensing transistors (232, 234) and transistor (308) of the temperature detection voltage generator are CMOS transistors.

Regarding claims 6, 7 and 11, figure 2 and 3 of Cyrusian show a temperature detection circuit comprising:

amplifier means (316) for receiving a band gap reference voltage (320) and a first voltage at node (328);

reference current generator means (312, 414, 318) for generating the first voltage and a reference voltage (V3 at node 322) in response to an output signal of the amplifier means 316 (note that amplifier 316 generates current I1 that creates a reference voltage (V3) at node 322);

temperature detection means (308, 304 and 232, 234 in figure 2) for generating a temperature detection voltage (V4) at node (324) in response to a temperature of the temperature detection circuit and the output signal (330) of the amplifier means (316); and

comparator means (306) for comparing the reference voltage signal (V3) with the temperature detection voltage signal to generate a temperature control signal (Vb2). Element (320) is a band gap reference voltage generator (col. 9, lines 32-32). The sensing transistors (232, 234) and transistor (308) of the temperature detection voltage generator are CMOS transistors.

Allowable Subject Matter

Claims 2-4, and 8-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 2-4, and 8-10 are objected to because reference US 6,697,205 fails to teach or fairly suggest a band gap reference voltage generator comprising first and second reference current units, an op-amp and first and second bipolar transistors as called for in claims 2 and

8; a reference current generator comprising a first PMOS transistor, first to third resistors as called for in claims 3 and 9 and a temperature detection voltage generator comprising a second PMOS transistor, fourth and fifth resistors and a diode connected PNP transistor as called for in claims 4 and 10.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep Nguyen

07-07-04

MY-TRANG NU TON
PRIMARY EXAMINER
07/08/04